Title of the Invention:

Post-Etch Clean Process for Porous Low Dielectric Constant Materials

Field of the Invention

[0001] The present disclosure is generally related to the field of semiconductor manufacturing, and more specifically to a method of removing volatile compounds from exposed dielectric material prior to metal deposition.

Background of the Invention

[0002] Semiconductor devices, such as microchip circuits, are typically formed through cycles of deposition, patterning and etching a semiconductor substrate or wafer. Photolithography is one available process by which a circuit pattern or other structure is formed on a wafer. Photoresist is a light-sensitive organic polymer that is used to develop a pattern which masks or protects some areas of the wafer during an etch process.

[0003] Wafer cleaning, particularly the removal of photoresist and post-etch polymers, has always been of paramount importance in achieving high quality devices in semiconductor manufacturing. Improper cleaning can lead to lower yields, manufacturing tool failure and reduced semiconductor device performance. Standard cleans are performed with known dry and/or wet clean processes. For example, standard post-etch clean procedures use a dry (plasma) clean to strip the photoresist followed by a wet (solvent or acid-based) clean to remove post-strip polymer residues. After one or more cleans are performed, the wafer then undergoes one or more metal deposition steps.

[0004] It has been found that certain components of wet clean solvents may inadvertently be absorbed into porous materials used in device processing during the wet clean process, particularly materials such as organosilicate glass (OSG), carbon-doped silicon-oxides (SiOC or CDO), or methylsilsesquioxane (MSQ). In many cases, these solvent components can volatilize during the subsequent metal deposition steps. Such components are not readily detectable following the wet clean through standard surface inspection by scanning electron microscope (SEM). However, these volatile components have been found to be present through the use of residual gas analyzers (RGA) during the metal barrier depositions and when not addressed, have resulted in the rejection and loss of entire production lots of post-etch wafers.

[0005] With the continued scaling of devices below 100 nanometers (nm) and the introduction of new semiconductor materials, standard wafer cleaning processes need to be refined in order to alleviate and prevent future failures or re-works and increase semiconductor device production yields. Accordingly, there is a need for an enhanced post-etch clean process that addresses certain problems of existing technologies.

Summary of the Invention

[0006] It is an object of the present disclosure, therefore, to present particular processes for cleaning an etched semiconductor wafer. Prior to a metal deposition step, the post-etch wafer may be subjected to one or more clean processes. For example, a plasma clean may be performed to remove a photoresist from the wafer. Remaining polymeric residue may then be removed using a wet clean process in which a standard solvent is applied.

[0007] Application of the solvent may cause one or more volatile solvent components or by-products to be inadvertently absorbed into the wafer structure. In order to effectively

remove such components, a high-temperature, low-pressure anneal of short duration is introduced after a wet clean process and prior to a metal deposition process, whereby the volatile compounds are substantially eradicated without affecting the critical dimension of the semiconductor structure or causing metal extrusion into etched features from underlying metal layers.

Brief Description of the Drawings

[0008] Further aspects of the present disclosure will be more readily appreciated upon review of the detailed description of its various embodiments, described below, when taken in conjunction with the accompanying drawings, of which:

[0009] FIG. 1 is a flow diagram of a post-etch wafer before and after a metal deposition.

Detailed Description of the Specific Embodiments

[0010] Referring now to FIG. 1, various features of a post-etch clean process for porous dielectric materials will now be described.

[0011] An etched wafer 100 includes a semiconductor substrate (not pictured) which forms the base layer upon which all active device structures and interconnection structures are built and which includes dielectric layer 102 and one or more underlying metal layers 104. In particular embodiments, the layer 102 may be made of a low-dielectric constant (k) material, such as OSG ($k \sim 2.7$), and the underlying metal layers 104 are made of copper (Cu). However, it should be readily appreciated that the dielectric material 102 may be any useful or known

organic or inorganic materials with varying k, such as fluorine-doped silicate glass (FSG), silicon-dioxide (SiO_2), or MSQ and known variants of these materials, including more porous versions of these materials. Available low-k (having k <=3.0) alternatives to OSG include, but are not limited to, MSQ-based, low-k porous dielectrics of the type developed by JSR CORPORATION (k ~ 2.2), APPLIED MATERIALS "BLACK DIAMOND" materials, or NOVELLUS CORPORATION CORAL OSG. It should also be readily understood that the underlying metal layers 104, as well as the metal used in subsequent metallization steps, may be any useful metal, such as aluminum (Al) and/ or copper.

[0012] The etched wafer 100 includes a via 106 and/or a trench 108 resulting from prior patterning and etch steps (not shown). The via 106 and trench 108 may result from any of a variety of known processing steps, including photolithography, in which a photoresist is applied to designate a pattern in a wafer that is subsequently etched. The formation of the interconnect wiring of an integrated circuit device may occur in accordance with various single damascene processes, in which vias and trenches are formed simultaneously, or dual damascene processes, in which the vias and the trenches are formed in separate etching steps. According to dual damascene practices, vias may be formed before trenches or vice-versa. Any of a variety of additional steps are performed to produce active device components as well as the interconnect wiring of the chip, during which time the etched wafer 100 is produced. Etch steps may include an etch-stop etch, a shallow trench isolation (STI)-etch, a gate-etch, a metal-etch and a contact-etch. One of skill in the art will readily appreciate that the etched wafer 100 is not limited to the exemplary structure depicted in FIG. 1 and, in fact, may be in any of a variety of forms useful for producing semiconductor devices.

[0013] After the etch steps are performed, the etched wafer 100 is subject to one or more clean processes to remove all undesirable materials from the surface of the wafer without causing damage to the wafer layers. Various wet clean and/or dry clean technologies may be used, and either may be repeated a number of times as needed. In particular embodiments, the etched wafer 100 may first be subjected to a dry clean process (not shown) to remove the photoresist after etching. The dry clean may include an application of a hydrogen (H) plasma and may further include H, oxygen (O), and/or an inert gas, such as argon (Ar), helium (He), neon (Ne), xenon (Xe) or some other inert gas, the plasma generated by applying radio frequency (RF) or microwave frequency radiation. In certain embodiments, a plasma strip (also referred to as photoresist removal or ashing) may be applied in a heated environment. The dry clean is performed for a limited duration, typically within the range of approximately 30 seconds to several minutes, depending on the resist thickness and the process used to remove it. The process must be of sufficient duration to effectively remove the photoresist without affecting a critical dimension (CD) of the semiconductor structure or causing metal extrusion of the underlying metal layers 104, which may happen particularly in devices with larger metal widths.

[0014] The dry clean typically leaves some polymeric residues on the surface of the layer 102. Accordingly, a wet clean process may next be performed, in which a solvent is applied to the surface of the layer 102 in order to remove the remaining residues. The solvent may be any standard wet clean solvent, including fluorine-based solvents or acids, and may include dimethyl acetamide (DMAC), such as those solvents commercially available from ASHLAND CORPORATION and other suppliers of semiconductor cleaning fluids. Particular wet clean processes, such as those involving wet benches, spin/rinse/dryers, and brush scrubbers may also be included.

[0015] In prior known semiconductor device manufacturing processes, the wet clean (or the last of a series of wet cleans) was the step immediately prior to a metal deposition step (such as a barrier deposition or a metal seed layer deposition) in which a metal 110 is deposited on the surface of the exposed dielectric layer 102. However, production lots which were analyzed by RGA during the barrier deposition process have occasionally failed due to high levels of organic material observed in the RGA trace coming from the wafer prior to the metal deposition step, and would accordingly have to be re-worked. It was initially assumed that the resist removal had not been complete. However, polymer residues were not detected in the failed lots by SEM inspection. The failed lots were sent back for a second H-plasma strip performed at 250°C for 45 seconds with a commercial asher. The re-worked lots were then tested to determine whether the lots were acceptable. Such re-worked lots passed RGA analysis. However, the use of RF power to generate the plasma for that short duration of 45 seconds resulted in undesirable OSG dielectric film loss and unwanted increases in CDs.

[0016] It was later determined that the wet clean solvent left a mass-to-charge (m/e) 59 component that was absorbed in the dielectric film layer 102. Such solvent components would volatilize during the barrier deposition step, resulting in later tool and device failures.

[0017] It was found that the volatile components were successfully removed, without affecting CD or causing metal extrusions, by performing an anneal of elevated temperature in a low pressure (from substantially one atmosphere of pressure to a substantial vacuum) environment for a limited duration of time. In practice, most such anneals may be limited in duration to at most three minutes, or may extend up to approximately six minutes dependent on the type of low-k material used. Longer durations could be employed if they do not adversely

affect device performance, but such durations are still generally limited to the scale of a few minutes.

[0018] The temperature must be above the boiling points of the major components of the solvent to remove the absorbed volatile components. However, the temperature must not be sufficiently high so as to effect device performance, such as by allowing passive extrusions.

[0019] It was found that, in the case of copper in the underlying metal layer 104 of an OSG etched wafer 100, the temperature should not exceed approximately 300° Celsius, in order to avoid such extrusions. In a particular embodiment, an anneal at 250° Celsius for a duration of 45 seconds was found to completely remove the absorbed components from OSG wafers, without the OSG film loss or copper extrusions resulting from the limited duration plasma re-work described previously.

[0020] The anneal may be performed in a furnace of suitable design to achieve the anneal parameters specified. The anneal may also be performed in an asher operated without applying RF or microwave radiation, but with the wafer held in the processing chamber at elevated temperature, and in less than one atmosphere pressure.

[0021] Although the best methodologies of the invention have been particularly described in the foregoing disclosure, it is to be understood that such descriptions have been provided for purposes of illustration only, and that other variations both in form and in detail can be made thereupon by those skilled in the art without departing from the spirit and scope of the present invention, which is defined first and foremost by the appended claims.